In the Claims:

1. (Currently Amended) A method of forming a resist layer on a non-planar surface of a substrate with protruding 3D structures, the method comprising:

providing a substrate having a non-planar surface with protruding 3D structures;

forming a layer of conductive material over the protruding 3D structures;

placing the non-planar surface, including the layer of conductive material, into an electrophoretic resist;

while the non-planar surface is in the electrophoretic resist, applying an electrical voltage between the substrate and the electrophoretic resist; and

removing the non-planar surface from the electrophoretic resist;

2. (Currently Amended) The method of claim 1 wherein the non-planar surface comprises a substantially planar surface ~~with a structure formed thereon~~ except for the protruding 3D structures.

3. (Currently Amended) The method of claim [[2]] 1 wherein the protruding 3D structure comprise[[s a]] compliant elements.

4. (Currently Amended) The method of claim 1 and further comprising:

~~forming a conductive layer over the non-planar surface prior to placing the non-planar surface in the electrophoretic resist; and~~

patterning the electrophoretic resist after removing the non-planar surface from the electrophoretic resist.

5. (Original) The method of claim 4 wherein the conductive layer comprises a seed layer, the method further comprising removing the electrophoretic resist from portions of the seed layer and forming a second conductive layer over portions of the seed layer not covered by the electrophoretic resist.

6. (Original) The method of claim 5 wherein forming a second conductive layer comprises:

forming a copper layer over portions of the seed layer not covered by the electrophoretic resist;

forming a nickel layer over the copper layer; and

forming a gold layer over the nickel layer.

7. (Original) The method of claim 5 wherein the substrate comprises a semiconductor wafer and wherein the second conductive layer comprises a reroute layer electrically coupling a contact pad formed on the semiconductor wafer to a terminal on the non-planar surface.

8. (Original) The method of claim 1 wherein the substrate includes a rear surface oppositely disposed from the non-planar surface, the method further comprising protecting the rear surface from wetting while the non-planar surface is placed in the electrophoretic resist.

9. (Original) The method of claim 1 and further comprising causing the non-planar surface to be moved relative to the electrophoretic resist while the non-planar surface is placed in the electrophoretic resist.

10. (Original) The method of claim 9 wherein the non-planar surface is rotated while the non-planar surface is placed in the electrophoretic resist.

11. (Original) The method of claim 9 wherein the electrophoretic resist is stirred while the non-planar surface is placed in the electrophoretic resist.

12. (Original) The method of claim 1 and further comprising heating the substrate after removing the non-planar surface from the electrophoretic resist.

13. (Original) A method for forming a plurality of three-dimensional structures on a substrate, the method comprising:

providing a wafer with bumps distributed on a surface of the wafer; and

forming a resist over the surface of the wafer including the bumps by coating the surface of the wafer with an electrophoretic resist by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic resist.

14. (Currently Amended) The method of claim 13 and further comprising:

patterning the resist to expose a seed layer over the surface of the wafer; and

forming a plurality of conductors over the exposed seed layer ~~surface of the wafer in accordance with the patterning~~.

15. (Original) The method of claim 14 wherein the plurality of conductors electrically connect bonding pads on the wafer to terminals located on the bumps.

16. (Original) The method of claim 13 wherein the surface of the wafer is dipped into the electrophoretic resist in a horizontal arrangement of the wafer.

17. (Original) The method of claim 16 wherein a rear side of the wafer is protected from wetting during the process of dipping into the electrophoretic resist.

18. (Original) The method of claim 13 wherein the wafer is caused to rotate during the coating operation.

19. (Original) The method of claim 13 wherein a flow is produced at least below the wafer in the electrophoretic resist during the coating operation.

20. (Original) The method of claim 19 wherein the electrophoretic resist is caused to rotate in a region of the surface of the wafer.

21. (Original) The method of claim 20 wherein the rotation of the electrophoretic resist is produced by a stirrer.

22. (Original) The method of claim 13 wherein the wafer is removed in a horizontal position after the process of coating with the electrophoretic resist and the coating is baked thermally.